REMARKS

Claims 1-26 are pending in this application.

Claims 1-6, 8, 9, 12-17 and 20-26 were rejected and Claims 7, 10, 11, 18 and 19 were objected to under 35 U.S.C. § 102. Claims 2 and 13 were amended to correct the British word "utilised" to "utilized".

Claim Rejections -- 35 U.S.C. § 102

Claims 1-6, 8-9, 12-17 and 20-26 were rejected as anticipated by *Mitsuishi, et al.* (USP 6,907,514, hereinafter "Mitsuishi"). Claims 7, 10-11 and 18-19 were objected to as being dependant upon a rejected base claim, but Examiner notes these claims would be allowable if re-written in independent form. These rejections are traversed.

Independent claim 1 requires, among other limitations,

> a request directing unit for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps, wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface, and in said second memory address map said first range of addresses are also allocated to the interface.

Nothing in Mitsuishi appears to teach or suggest this limitation. The portion of Mitsuishi cited in the Office Action for this limitation is concerned with Figure 4, which depicts a typical address decoding circuit. Here Mitsuishi does describe determining whether the decoded address

points to an internal address bus and related devices or to a component in the external space.

Nothing in this portion describes the claimed first and second address maps, and the allocation of address ranges therein. Mitsuishi's Figure 2 does depict address maps, but the accompanying description in col. 13, line 62 – col. 14, line 38 includes no teaching or suggestion of a first address map having a first range of addresses allocated to at least one on-chip resource and a second range of addresses allocated to an interface for directing packets off-chip, and a second memory address map where the first range of addresses are also allocated to the interface, as required by claim 1.

Neither does any other cited art include such a teaching or suggestion.

Independent claim 12 requires, among other limitations,

> a request directing unit for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps, wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface, and in the second memory address map said first range of addresses are also allocated to the interface; and an off-chip circuit connected to said interface and including at least one off-chip memory resource.

Claim 12 therefore contains limitations similar to those of claim 1, and the arguments with respect to claim 1 apply. Mitsuishi does not teach or suggest these limitations.

Independent claim 20 requires, among other limitations,

> in accordance with a selected mode of operation, selectively supplying said memory access requests to at least one of said first and second memory address maps, and directing the memory access requests selectively to said on-chip memory resource or said off-chip circuit in dependence on the selected one of said first and second address maps

These limitations are not taught or suggested by the art of record. Mitsuishi does appear to depict, in Figure 4, a "MODE" selector that would appear to have some impact on memory addressing, but Mitsuishi contains no description at all of the MODE selector or what effect it has. Certainly, it does not appear to function as a means for selectively supplying memory access requests to at least one of the first and second memory address maps.

As each of the independent claims contains limitations not taught or suggested by Mitsuishi, these anticipation rejections, and those of all dependent claims, are traversed. Reconsideration and allowance are respectfully requested.

SUMMARY

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is authorized to charge any fees connected with this communication (including any extension of time fees) or credit any overpayment to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

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